ABSTRACT OF THE DISCLOSURE

A method for producing a liner mask on a semiconductor structure is disclosed. The method may include providing an amorphous liner layer (55) on the top side (OS;OS') of the semiconductor structure, annealing the amorphous liner layer (55) to increase the crystallisation and generate a semi-crystalline liner layer (55); implanting (I1) extrinsic ions in a subregion (55a) of the semi-crystalline liner layer (55) to decrease the etching rate of the subregion (55a) and create an etch selectivity between the to the subregion (55a) complementary subregion (55b) and the subregion (55a) in the predetermined etchant; and selectively removing of the to the subregion (55a) complementary subregion (55b) opposite to the subregion (55a) in a etching step in the predetermined etchant for completing the liner mask.